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10/717,593	11/19/2003	Sealtiel Avalos	22768.21	8685

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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/717,593	AVALOS ET AL.	
	Examiner	Art Unit	
	Jason R. Kurr	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4/28/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-6, 11-14 and 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Richards (US 4,907,082) in view of Gibson (US 4,747,140).

With respect to claim 1, Richards discloses a decoding system for demodulating a modulated analog signal containing a L+R signal, a L-R signal centered around a carrier signal, and a pilot signal (col.2 ln.33-65), the system comprising: first (fig.1 #29), second (fig.1 #30), and third (fig.1 #27) filters adapted to separate the L+R signal, the pilot signal, and the L-R signal, respectively, from the signal (col.3 ln.17-29); clock reconstitution circuitry adapted to reconstitute a clock signal from the pilot signal (fig.1 #31,35); L-R signal recovery circuitry (fig.1 #30,39) adapted to recover the L-R signal using the reconstituted clock signal (col.3 ln.23-29); and channel recovery circuitry (fig.1 #41) adapted to recover a left channel signal and a right channel signal from the L+R signal and the L-R signal (col.3 ln.43-49).

Richards does not disclose expressly wherein the decoding system **digitally** demodulates the modulated analog signal wherein an analog to digital converter is

adapted to convert the analog signal into a digital signal and the first, second and third filters are digital.

Gibson discloses a decoding system that digitally demodulates a modulated MTS signal (fig.2, col.2 ln.9-23) wherein an analog to digital converter (fig.2 #12) is adapted to convert the analog signal into a digital signal and the first, second and third filters (fig.2 #14,16,18) are digital.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use a digital demodulating setup in the system of Richards as implemented by Gibson.

The motivation for doing so would have been to reduce the number of parts needed to implement the circuit of Richards, because many of the circuit elements depicted in figure 1 of Richards may be implemented on a digital signal processor.

With respect to claim 2, Richards discloses the digital decoding system of claim 1 wherein the first digital filter is a low pass filter (fig.1 #29), however does not disclose expressly wherein the second digital filter is a bandpass filter, and the third digital filter is a high pass filter.

Official Notice is taken that it is well known in the art to filter signals to a desired frequency range. The transmission/carrier frequencies set for MTS signals by the BTSC are also well known in the art as evidenced by figures 1 and 1a of Gibson and Richards. At the time of the invention it would have been obvious to a person of ordinary skill in the art to use appropriate filters, such as a BPF for the pilot signal and a HPF for the L-R signal, to separate the desired signals from the input composite signal.

The motivation for filtering the signals to the frequency range set by the BTSC would have been to exclude any high frequency noises that are common to signal transmission.

With respect to claim 3, Richards discloses the digital decoding system of claim 2 wherein the low pass filter has a cut-off frequency of approximately 13.8 kHz, the band pass filter is centered at approximately 15.734 kHz, and the high pass filter is adapted to remove frequencies that pass through the low pass and band pass filters (col.2 ln.39-53).

With respect to claim 4, Richards discloses the digital decoding system of claim 2 further comprising additional signal recovery circuitry (fig.1 #35) including a demodulator adapted to receive input from the clock reconstitution circuitry and the high pass filter (col.3 ln.31-42), wherein the additional signal recovery circuitry is adapted to recover a signal (fig.1 "SAP") other than the L+R signal, L-R signal, and pilot signal from the modulated analog signal.

With respect to claim 5, Richards discloses the digital decoding system of claim 4 wherein the additional signal is a second audio program (SAP) signal (col.3 ln.31-42).

With respect to claim 6, Richards discloses the digital decoding system of claim 2 wherein the L-R signal recovery circuitry includes: a synchronous demodulator (fig.1 #30) adapted to demodulate the L-R signal received from the high pass filter using clock information from the clock reconstitution circuitry (col.3 ln.17-29); and an expander (fig.1 #39) for expanding the demodulated L-R signal (col.3 ln.34-41).

With respect to claim 11, Richards discloses the digital decoding system of claim 1 wherein the channel recovery circuitry is adapted to calculate a sum and a difference of the L+R signal and the L-R signal (col.3 ln.42-56).

With respect to claim 12, Richards discloses the digital decoding system of claim 1 in view of Gibson, further comprising a digital to analog converter adapted to convert the recovered left channel and right channel signals from digital signals into analog signals (Gibson: fig.2 #36).

With respect to claim 13, Richards discloses a demodulator for demodulating a received analog signal including having a pilot signal, a L+R signal, and a L-R signal (col.2 ln.33-65), the demodulator comprising: a plurality of filters (fig.1 #27,29,33) for separating the pilot signal, L+R signal, and L-R signal into a clock reconstitution path, a L+R signal path, and a L-R signal path (fig.1), respectively; circuitry within the clock reconstitution path for reconstituting a clock signal from the pilot signal (fig.1 #31); circuitry within at least one of the L+R and L-R signal paths for recovering at least one of the L+R or L-R signals using the reconstituted clock signal (fig.1 #30); and circuitry for recovering a Left signal and a Right signal from the L+R signal path and the L-R signal path (fig.1 #41).

Richards does not disclose expressly wherein the decoding system **digitally** demodulates the modulated analog signal wherein an analog to digital converter is adapted to convert the analog signal into a digital signal.

Gibson discloses a decoding system that digitally demodulates a modulated MTS signal (fig.2, col.2 ln.9-23) wherein an analog to digital converter (fig.2 #12) is adapted to convert the analog signal into a digital signal.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use a digital demodulating setup in the system of Richards as implemented by Gibson.

The motivation for doing so would have been to reduce the number of parts needed to implement the circuit of Richards, because many of the circuit elements depicted in figure 1 of Richards may be implemented on a digital signal processor.

With respect to claim 14, Richards discloses the demodulator of claim 13 wherein the circuitry for recovering the Left and Right signals includes a demultiplexing matrix (fig.1 #41).

With respect to claim 18, Richards discloses a method for decoding an encoded signal, the method comprising: receiving an encoded signal from a single analog channel (fig.1 #1), wherein the encoded signal includes at least first and second audio signals (col.2 ln.33-65); separating the converted signal using multiple filters (fig.1 #27,29,33) into first and second signal paths for the first and second audio signals, respectively, and a clock reconstitution path; and recovering the first and second audio signals using the first and second signal paths, respectively, wherein at least one of the first and second audio signals is recovered based on information from the clock reconstitution path (fig.1 #31,35, col.3 ln.17-29).

Richards does not disclose expressly wherein the decoding method **digitally** decodes the encoded analog signal wherein an analog to digital converter is adapted to convert the analog signal into a digital signal and the multiple filters are digital.

Gibson discloses a decoding system that digitally demodulates a modulated MTS signal (fig.2, col.2 ln.9-23) wherein an analog to digital converter (fig.2 #12) is adapted to convert the analog signal into a digital signal and the multiple filters (fig.2 #14,16,18) are digital.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use a digital demodulating setup in the system of Richards as implemented by Gibson.

The motivation for doing so would have been to reduce the number of parts needed to implement the circuit of Richards, because many of the circuit elements depicted in figure 1 of Richards may be implemented on a digital signal processor.

With respect to claim 19, Richards discloses the method of claim 18 in view of Gibson, further comprising performing a digital to analog conversion on the two recovered audio signals (Gibson: fig.2 #36).

With respect to claim 20, Richards discloses the method of claim 18 wherein recovering at least one of the first and second audio signals includes reconstituting clock information carried within the received signal (col.3 ln.17-29).

Claims 7-8, 10 and 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Richards (US 4,907,082) in view of Gibson (US 4,747,140) and in further view of Scarpa et al (US 5,673,293).

With respect to claim 7, Richards discloses the digital decoding system of claim 1 wherein the clock reconstitution circuitry comprises a phase-locked loop (PLL) (fig.1 #31, col.3 ln.17-29), however does not disclose expressly wherein the PLL is associated with at least one lookup table.

Scarpa discloses a digital decoding system for demodulating analog signals wherein a PLL is associated with a lookup table (col.9 ln.53-67, col.10 ln.1-5).

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use the lookup table of Scarpa to generate a sin/cos signal for use by the L-R demodulator of Richards.

The motivation for doing so would have been to precisely recreate the L-R signal through the use of a predefined table of signal parameters.

With respect to claim 8, Richards discloses the digital decoding system of claim 7 in view of Scarpa, wherein an output of the PLL represents a phase of the pilot signal, and wherein the output is used to address the lookup table to generate a sine wave for the L-R signal recovery circuitry (Scarpa: col.9 ln.53-67, col.10 ln.1-5).

With respect to claim 10, Richards discloses the digital decoding system of claim 7 wherein the PLL includes a sample rate of approximately 24 MHz. It is implied that the PLL of Richards samples data at a sufficient rate, such as 24 MHz, in order to update

the generation of the sin/cos signal for the purpose of accurately demodulating the L-R signal.

With respect to claim 15, Richards discloses the demodulator of claim 13 wherein the circuitry within the clock reconstitution path includes a phase-locked loop (PLL) (fig.1 #31), however does not disclose expressly wherein the PLL is associated with at least a first lookup table, or wherein the PLL is adapted to generate a digital value that is compared to a plurality of digital values in the first lookup table for use in at least one of the L+R and L-R signal paths.

Scarpa discloses a digital decoding system for demodulating analog signals wherein a PLL is associated with a lookup table (col.9 ln.53-67, col.10 ln.1-5).

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use the lookup table of Scarpa to generate a sin/cos signal for use by the L-R demodulator of Richards.

The motivation for doing so would have been to precisely recreate the L-R signal through the use of a predefined table of signal parameters.

With respect to claim 16, Richards discloses the demodulator of claim 15 further comprising additional signal recovery circuitry (fig.1 #35) adapted to recover a signal other than the L+R signal, L-R signal, and pilot signal (fig.1 "SAP").

With respect to claim 17, Richards discloses the demodulator of claim 16 in view of Scarpa, wherein the circuitry within the clock reconstitution path includes a second lookup table for use with the additional signal recovery circuitry.

Scarpa discloses a digital decoding system for demodulating analog signals wherein a PLL is associated with a lookup table (col.9 ln.53-67, col.10 ln.1-5).

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use a second lookup table to generate a sin/cos signal for use by the L-R demodulator of Richards when a user selects the secondary audio program signal (SAP).

The motivation for doing so would have been to precisely recreate the SAP signal through the use of a predefined table of signal parameters.

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Richards (US 4,907,082) in view of Gibson (US 4,747,140) in view of Scarpa et al (US 5,673,293) and in further view of Elliott et al (US 6,826,247 B1).

With respect to claim 9, Richards discloses the digital decoding system of claim 7, however does not disclose expressly wherein the PLL comprises a digital phase accumulator and a second order accumulator.

Elliott discloses a PLL comprising a digital phase accumulator (fig.2 #208) and a second order accumulator (col.13 ln.31-44).

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use the digital PLL of Elliott in the system of Richards.

The motivation for doing so would have been to reduce input jitter noise by driving the phase error to zero through the use of Elliott's second order PLL system.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Wu et al (US 2003/0161477 A1) discloses a system and method of performing digital multi-channel audio signal decoding.

Ingram et al (US 5,428,404) discloses an apparatus for selectively demodulating and remodulating alternate channels of a television broadcast.

Kim (US 5,337,196) discloses a tape recorder with an audio decoder.

Zink (US 4,757,538) discloses separation of L+R from L-R in BTSC system.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason R. Kurr whose telephone number is (571) 272-0552. The examiner can normally be reached on M-F 10:00am to 6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vivian Chin can be reached on (571) 273-7848. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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